In the outstanding Office Action, the Examiner rejected claims 14-39 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,720,257 to Shin and U.S. Patent No. 6,025,635 to Kirvokapic, and further in view of U.S. Patent No. 6,228,763 to Lee.

To establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. (See M.P.E.P. §2143.03 (8th ed. 2001)). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." (M.P.E.P. §2143 (8th ed. 2001)).

The Examiner's rejection of claims 14-39 under § 103 fails to meet these requirements, as set forth below.

Shin discloses in Figs. 3A and 3B forming a nitride layer 22 on a substrate 21, etching a portion of the nitride layer 22 to form a mask, and then etching the substrate 21 to form a trench (col. 4, lines 15-27). Fig. 3B further shows a gate oxide layer 23 is grown on the exposed trench surface of the substrate 21 and the nitride layer 22 (col. 4, lines 30-32). A polysilicon gate 24 is formed in the trench, and the silicon substrate 21 is doped to form source 26a and drain 26b (Fig. 3C, col. 4, lines 40-47).

As shown in Fig. 3C, a bottom surface of source 26a and drain 26b is higher than the bottom surface of the trench. Hence, to the extent source 26a or drain 26b may

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correspond to the impurity diffusion region, Shin does not disclose an "impurity diffusion region including a part of a bottom of the first groove," as recited in independent claims 14 and 18, for example. Since both regions 26a and 26b are higher than the bottom surface of the trench, they cannot include the bottom part of the first groove.

In addition, Shin does not even disclose "a second film" or a "gate insulator film", as recited in claims 14 and 18, let alone the other recitations relating to the second film or gate insulator film. For instance, nothing in Shin discloses the following limitations of claims 14 and 18: "using the second film as a mask," "removing the second film to form a second groove," and "forming a gate insulator film in the second groove ... so that a top surface of the gate insulator film is arranged higher than a top surface of the gate insulator film." The Examiner appears to characterize gate electrode 24 as the claimed second film. That characterization is improper, however, since gate electrode 24 is not "us[ed] as a mask" or "remov[ed] to form a second groove," as recited in claims 14 and 18. Further, by characterizing Shin in this way, the Examiner cannot then point to the disclosure in Shin that teaches the recitation in claims 14 and 18 of "forming a gate electrode on the top of the gate insulator film" or the gate insulating film.

Krivokapic also does not cure the deficiencies of Shin noted above. Contrary to the statement made by the Examiner, col. 6, lines 15-27 and Figs. 8 and 9 of Krivokapic do not teach the recitations forming an "insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove," as recited in claims 14 and 18. This passage of Kirvokapic describes forming spacers 215 using Figs. 7 and 8 for illustration.

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Fig. 7 of Krivokapic teaches forming a gate region 190 by removing an oxide layer 75 and oxide spacer 110, and forming an oxide layer 205 along gate region sidewalls 195 and on a epitaxial lateral overgrowth layer 185 (col. 6, lines 5-14). Fig. 7 further teaches removing nitride layer 70 to form oxide region 200 on the bottom of gate region 190 (col. 6, lines 14-16). Thus, Krivokapic teaches forming a gate region or trench 190 having oxide sidewalls 195 and an oxide layer 200 at the bottom. Fig. 8 of Krivokapic further teaches forming adaptively controlled spacers 215 in gate region 190 (col. 6, lines 19-21), and Fig. 9 discloses etching oxide layer 200 to leave a minor portion of the oxide layer 200a under spacers 215 for support.

Thus, Krivokapic does not teach an "impurity diffusion region including a bottom of the first groove," or any of the steps recited in claims 14 and 18, such as "etching said semiconductor substrate to form a first groove by using said first film as a mask," "diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including a part of a bottom of said first groove by using said second film as a mask," and "forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove."

Independent claims 14, 18, 22, and 27 and dependent claim 33 each recite a gate insulator film having a top surface higher than a top surface of the impurity diffusion region. As described above, Shin does not even disclose a gate insulator film, let alone that a "top surface of the gate insulator film is higher than a top surface of the impurity diffusion region," as recited in claims 14, 18, 22, 27, and 33. Kirvokapic and Lee also do not disclose a gate insulator film. Accordingly, claims 14, 18, 22, 27, and

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33 are patentable. Claims 15-17, 19-21, 23-26, and 28-31 are patentable as well, at least in view of their dependence from allowable claims 14, 18, 22, and 27, respectively.

With respect to claim 32, none of the cited references disclose or suggest "selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor substrate and said channel region." The Examiner asserts that the incline on regions 26a and 26b in Fig. 3E of Shin discloses this feature. However, the inclined 26a and 26b in Shin is not formed between the top surface of said semiconductor substrate and said channel region, as recited in claim 32. Lee and Kirvokapic also fail to teach the structure recited in claim 32. Accordingly, at least for this reason, claim 32 is patentable.

Applicants respectfully request that this Amendment under 37 C.F.R. § 1.116 be entered by the Examiner, placing claims 14-39 (35-39 cancelled) in condition for allowance. Applicants submit that the proposed amendments of claims 14, 18, 22, 27, 32, and 33 do not raise new issues or necessitate the undertaking of any additional search of the art by the Examiner, all of the elements and their relationships claimed were either earlier claimed or inherent in the claims as examined. Therefore, this Amendment should allow for immediate action by the Examiner.

Furthermore, Applicants respectfully point out that the final action by the Examiner presented some new arguments as to the Examiner's application of the art against the pending claims. It is respectfully submitted that the entering of the Amendment would allow the Applicants to reply to the final rejection and thus place the application in condition for allowance.

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Finally, Applicants submit that the entry of the amendment would place the application in better form for appeal, should the Examiner dispute the patentability of the pending claims.

CONCLUSION

Attached hereto is a marked-up version of the changes made to the claims by this amendment. The attachment is captioned "**Appendix to the Amendment After Final of September 3, 2002**" Deletions appear as normal text surrounded by [ ] and additions appear as underlined text.

In view of the foregoing, Applicants submit that claims 14-33, as amended, are neither anticipated nor rendered obvious in view of the prior art references cited against this application. Applicants therefore request the entry of this Amendment, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 3, 2002

By: Tara Bleech
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APPENDIX TO AMENDMENT AFTER FINAL OF SEPTEMBER 3, 2002

Version with Markings to Show Changes Made

Amendments to the Claims

Please amend claims 14, 18, 22, 27, 32, and 33, and cancel claims 34-39 without prejudice or disclaimer, as follows:

14. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the semiconductor substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity on a surface of said semiconductor substrate to form an [grooved] impurity diffusion region including a part of a bottom of said first groove by using said second film as a mask;

forming an insulator film on said [grooved] impurity diffusion region and thereafter removing said second film to form a second groove;

forming a gate insulator film in said second groove so that a top surface of said gate insulator film is higher [arranged farther from said semiconductor substrate] than a top surface of said [grooved] impurity diffusion region; and

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forming a gate electrode on the top surface of said gate insulator film.

18. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the semiconductor substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity on a surface of said semiconductor substrate to form an [grooved] impurity diffusion region including a part of a bottom of said first groove by using said second film as a mask;

forming an insulator film on said [grooved] impurity diffusion region and thereafter removing said second film to form a second groove;

forming a gate insulator film in said second groove and on said insulator film;

polishing said gate insulator film by using said insulator film as a stopper so that a top surface of said gate insulator film is [arranged farther from said semiconductor substrate] higher than a top surface of said [grooved] impurity diffusion region; and

forming a gate electrode on the top surface of said gate insulator film.

22. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate

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electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

diffusing an impurity on a surface of said semiconductor substrate to form an [grooved] impurity diffusion region including an elevated impurity diffusion region from a channel region by using said first film as a mask;

forming an insulator film on said [grooved] impurity diffusion region;

removing said first film so as to form a groove;

forming a gate insulator in said groove so that a top surface of said gate insulator film is [arranged farther from said semiconductor substrate] higher than a top surface of said [grooved] impurity diffusion region; and

forming a gate electrode on a top surface of said gate insulator film.

27. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

diffusing an impurity on a surface of said semiconductor substrate to form an [grooved] impurity diffusion region including an elevated impurity diffusion region from a channel region by using said first film as a mask;

forming an insulator film on said [grooved] impurity diffusion region;

removing said first film so as to form a groove;

forming a gate insulator in said groove and on said insulator film;

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polishing said gate insulator film by using said insulator film as a stopper so that a top surface of said gate insulator film is [arranged farther from said semiconductor substrate] higher than a top surface of said grooved impurity diffusion region; and

forming a gate electrode on a top surface of said gate insulator film.

32. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

forming a dummy film on said channel region, which borders said source drain regions;

selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor [layers] substrate and said channel region;

[forming a dummy film on said channel region, which borders said semiconductor layers;]

diffusing an impurity on a surface of said semiconductor substrate to form impurity diffusion regions by using said dummy film as a mask and thereafter removing said dummy film;

depositing an insulator film on an exposed surface of said channel region to form a gate insulator film, which has a cross section of a grooved space at a center thereof; and

depositing a gate electrode on a top of said gate insulator film to form a gate electrode having a cross section of a T shape.

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33. (Amended) A method for producing a MIS transistor according to claim 32, further comprising forming a gate insulator film from said insulator film in said second groove so that a top surface of said gate insulator film is [arranged farther from said semiconductor substrate] higher than a top surface of said grooved impurity diffusion region.

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